What is claimed is:

1. A three-terminal semiconductor transistor device, comprising:
   a) a base region formed by a semiconductor material of a first conductivity type at a first concentration, the base region being in contact with a first electrical terminal via a semiconductor material of the second conductivity type at a second concentration that is lower than the first concentration;
   b) a conductive emitter region in contact with the semiconductor base region, forming a first Schottky barrier junction at the interface of the conductive emitter region and the semiconductor base region, the conductive emitter region being in contact with a second electrical terminal; and
   c) a conductive collector region in contact with the semiconductor base region, forming a second Schottky barrier junction at the interface of the conductive collector region and the semiconductor base region, the conductive collector region being in contact with a third electrical terminal,

   wherein the tunneling current through the first Schottky barrier junction or the second Schottky barrier junction is substantially controlled by the voltage of the semiconductor base region.

2. The three-terminal semiconductor transistor device of claim 1 wherein the second conductivity type is the same as the first conductivity type.

3. The three-terminal semiconductor transistor device of claim 1 wherein the second conductivity type is the opposite of the first conductivity type.

4. The three-terminal semiconductor transistor device of claim 1 wherein the first concentration of the base region is above 10^{18} cm^{-3}.

5. The three-terminal semiconductor transistor device of claim 1 wherein the second concentration of the semiconductor material connecting the base region to the first electrical terminal is below 10^{18} cm^{-3}.

6. The three-terminal semiconductor transistor device of claim 1 wherein the first conductivity type is n-type or p-type.

7. The three-terminal semiconductor transistor device of claim 1 wherein the base region is not separated from the conductive emitter region or the conductive collector region by a continuous layer of insulating material.

8. The three-terminal semiconductor transistor device of claim 1 wherein the conductive emitter region or the collector region comprises one or more of metals, silicides, or metal compounds.

9. The three-terminal semiconductor transistor device of claim 1 wherein the conductive emitter region or the collector region comprises one or more of W, Ti, Ta, Mo, Pt, $TiSi_2$, $CoSi_2$, $NiSi_2$, WSi_2, $TaSi_2$, $MoSi_2$, PtSi, $TaSi_2$, $CrSi_2$, $RhSi_2$, and TiN.

10. The three-terminal semiconductor transistor device of claim 1 wherein the base region comprises a semiconductor selected from the group of silicon, germanium, and compound semiconductors.

11. The three-terminal semiconductor transistor device of claim 1 wherein the n-channel Schottky-barrier tunneling transistor is turned on by applying a positive voltage to the base region.

12. The three-terminal semiconductor transistor device of claim 1 wherein the barrier height for electrons at the first Schottky barrier junction of the n-channel Schottky-barrier tunneling transistor is between 0.01 eV and 1.12 eV.

13. The three-terminal semiconductor transistor device of claim 1 wherein the base region is n-type doped, forming an n-channel Schottky-barrier tunneling transistor.

14. The three-terminal semiconductor transistor device of claim 1 wherein the p-channel Schottky-barrier tunneling transistor is turned on by applying a negative voltage to the base region.

15. The three-terminal semiconductor transistor device of claim 1 wherein the barrier height for holes at the first Schottky barrier junction of a p-channel Schottky-barrier tunneling transistor is between 0.01 eV and 1.12 eV.

16. The three-terminal semiconductor transistor device of claim 1 wherein the base region is p-type doped, forming a p-channel Schottky-barrier tunneling transistor.

17. The three-terminal semiconductor transistor device of claim 1 wherein the conductive emitter region and the conductive collector region comprise the same material.

18. The three-terminal semiconductor transistor device of claim 1 wherein the Fermi level of the conductive emitter region or the conductive collector region is between the conduction band edge and the valence band edge of the semiconductor base region at thermal equilibrium.

19. The three-terminal semiconductor transistor device of claim 1 wherein the Fermi level of the conductive emitter region or the conductive collector region is below the mid band gap of the semiconductor base region at thermal equilibrium.

20. A three-dimensional three-terminal semiconductor device, comprising:
   a) a first insulating substrate layer; and
   b) a second substrate layer formed above the first insulating substrate layer, comprising:
      i) a base region formed by a semiconductor material of a first conductivity type at a first concentration, the base region being in contact with a first electrical terminal via a semiconductor material of the second conductivity type at a second concentration that is lower than the first concentration;
      ii) a conductive emitter region in contact with the semiconductor base region, forming a first Schottky barrier junction at the interface of the conductive emitter region and the semiconductor base region, the conductive emitter region being in contact with a second electrical terminal; and
      iii) a conductive collector region in contact with the semiconductor base region, forming a second Schottky barrier junction at the interface of the conductive collector region and the semiconductor base region, the conductive collector region being in contact with a third electrical terminal,

   wherein the tunneling current through the first Schottky barrier junction or the second Schottky barrier junction is substantially controlled by the voltage of the semiconductor base region.

21. The three-terminal semiconductor transistor device of claim 20 wherein the second electrical terminal is in contact with the sidewall or the top surface of the portion of the second substrate layer comprising the emitter region.

22. The three-terminal semiconductor transistor device of claim 20 wherein the third electrical terminal is in contact with the sidewall or the top surface of the portion of the second substrate layer comprising the collector region.

23. The three-terminal semiconductor transistor device of claim 20 wherein the second conductivity type is the same as the first conductivity type.

24. The three-terminal semiconductor transistor device of claim 20 wherein the second conductivity type is the opposite of the first conductivity type.

25. The three-terminal semiconductor transistor device of claim 20 wherein the first concentration of the base region is above 10^{18} cm^{-3}.

26. The three-terminal semiconductor transistor device of claim 20 wherein the second concentration of the semiconductor material connecting the base region to the first electrical terminal is below 10^{18} cm^{-3}.

27. The three-terminal semiconductor transistor device of claim 20 wherein the first conductivity type is n-type or p-type.

28. The three-terminal semiconductor transistor device of claim 20 wherein the base region is not separated from the conductive emitter region or the conductive collector region by a continuous layer of insulating material.

29. The three-dimensional three-terminal semiconductor device of claim 20, further comprising a substrate below the first insulating layer.

30. The three-dimensional three-terminal semiconductor device of claim 20, wherein the width of the base region is controlled by the encroachment of the silicidation process.

31. The three-dimensional three-terminal semiconductor device of claim 20, wherein the width of the base region is less than 1000 Å.

32. The three-dimensional three-terminal semiconductor device of claim 20, wherein the base region is formed in the single crystal silicon layer of a silicon-on-insulator (SOI) wafer.